AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph that begins on page 1, line 3, with the following:

[0001] This application claims priority to U.S. Provisional Application Serial No. 60/400,391 titled "JSM Protection," filed Jul. 31, 2002, incorporated herein by reference. This application also claims priority to EPO Application No. 03291906.0, filed Jul. 30, 2003 and entitled "Memory Management Of Local Variables," incorporated herein by reference. This application also may contain subject matter that may relate to the following commonly assigned co-pending applications incorporated herein by reference: "System And Method To Automatically Stack And Unstack Java Local Variables," Serial No. [[_____]] 10/632,228, filed Jul. 31, 2003~~, Attorney Docket No. TI-35422 (1962-05401)~~; "Memory Management Of Local Variables Upon A Change Of Context," Serial No. [[_____]] 10/632,076, filed Jul. 31, 2003~~, Attorney Docket No. TI-35424 (1962-05403)~~; "A Processor With A. Split Stack," Serial No. [[_____]] 10/632,079, filed Jul. 31, 2003~~, Attorney Docket No. TI-35425(1962-05404)~~; "Using IMPDEP2 For System Commands Related To Java Accelerator Hardware," Serial No. [[_____]] 10/632,069, filed Jul. 31, 2003~~, Attorney Docket No. TI-35426 (1962-05405)~~; "Test With Immediate And Skip Processor Instruction," Serial No. [[_____]] 10/632,214, filed Jul. 31, 2003~~, Attorney Docket No. TI-35427 (1962-05406)~~; "Test And Skip Processor Instruction Having At Least One Register Operand," Serial No. [[_____]] 10/632,084, filed Jul. 31, 2003~~, Attorney Docket No. TI-35248 (1962-05407)~~; "Synchronizing Stack Storage," Serial No. [[_____]] 10/631,422, filed Jul. 31, 2003~~, Attorney Docket No. TI-35429 (1962-05408)~~; "Methods And Apparatuses For Managing Memory," Serial No. [[_____]] 10/631,252, filed Jul. 31, 2003~~, Attorney Docket No. TI-35430 (1962-05409)~~; "Write Back Policy For Memory," Serial No. [[_____]] 10/631,185, filed Jul. 31, 2003~~, Attorney Docket No. TI-35431 (1962-05410)~~; "Methods And Apparatuses For Managing Memory," Serial No. [[_____]] 10/631,205, filed Jul. 31, 2003~~, Attorney Docket No. TI-35432 (1962-05411)~~; "Mixed Stack-Based RISC

Processor," Serial No. [[_____]]10/631,308, filed Jul. 31, 2003~~, Attorney Docket No. TI-35433 (1962-05412)~~; "Processor That Accommodates Multiple Instruction Sets And Multiple Decode Modes," Serial No. [[_____]]10/631,246, filed Jul. 31, 2003~~, Attorney Docket No. TI-35434 (1962-05413)~~; "System To Dispatch Several Instructions On Available Hardware Resources," Serial No. [[_____]]10/631,585, filed Jul. 31, 2003~~, Attorney Docket No. TI-35444 (1962-05414)~~; "Micro-Sequence Execution In A Processor," Serial No. [[_____]]10/632,216, filed Jul. 31, 2003~~, Attorney Docket No. TI-35445 (1962-05415)~~; "Program Counter Adjustment Based On The Detection Of An Instruction Prefix," Serial No. [[_____]]10/632,222, filed Jul. 31, 2003~~, Attorney Docket No. TI-35452 (1962-05416)~~; "Reformat Logic To Translate Between A Virtual Address And A Compressed Physical Address," Serial No. [[_____]]10/631,215, filed Jul. 31, 2003~~, Attorney Docket No. TI-35460 (1962-05417)~~; "Synchronization Of Processor States," Serial No. [[_____]]10/631,024, filed Jul. 31, 2003~~, Attorney Docket No. TI-35461 (1962-05418)~~; "Conditional Garbage Based On Monitoring To Improve Real Time Performance," Serial No. [[_____]]10/631,195, filed Jul. 31, 2003~~, Attorney Docket No. TI-35485 (1962-05419)~~; "Inter-Processor Control," Serial No. [[_____]]10/631,120, filed Jul. 31, 2003~~, Attorney Docket No. TI-35486(1962-05420)~~; "Cache Coherency In A Multi-Processor System," Serial No. [[_____]]10/632,229, filed Jul. 31, 2003~~, Attorney Docket No. TI-35637 (1962-05421)~~; "Concurrent Task Execution In A Multi-Processor, Single Operating System Environment," Serial No. [[_____]]10/632,638, filed Jul. 31, 2003~~, Attorney Docket No. TI-35638 (1962-05422)~~; and "A Multi-Processor Computing System Having A Java Stack Machine And A RISC-Based Processor," Serial No. [[_____]]10/631,939, filed Jul. 31, 2003~~, Attorney Docket No. TI-35710 (1962-05423)~~.

Please replace the paragraph that begins on page 11, line 11, with the following:

[0028] The data storage 122 generally comprises data cache ("D-cache") 124 and a data random access memory ("D-RAMset") 126. Reference may be made to copending applications U.S. Ser.

Nos. 09/591,537 filed Jun. 9, 2000 ~~(atty docket TI 29884)~~, 09/591,656 filed Jun. 9, 2000 ~~(atty docket TI 29960)~~, and 09/932,794 filed Aug. 17, 2001 ~~(atty docket TI 31351)~~, all of which are incorporated herein by reference. The stack (excluding the micro-stack 146), arrays and non-critical data may be stored in the D-cache 124, while Java local variables and associated pointers as explained below, as well as critical data and non-Java variables (e.g., C, C++) may be stored in D-RAMset 126. The instruction storage 130 may comprise instruction RAM ("I-RAMset") 132 and instruction cache ("I-cache") 134. The I-RAMset 132 may be used to store "complex" micro-sequenced Bytecodes or micro-sequences or predetermined sequences of code. The I-cache 134 may be used to store other types of Java Bytecode and mixed Java/C-ISA instructions.